

REMARKS

Claims 1-28 are currently pending in the subject application, and are presently under consideration. Claims 1-16 and 18-28 have been provisionally rejected. Claims 1-6, 11-18 and 20-28 are rejected. Claims 7-10 and 19 have been indicated as allowable. Claim 13 has been objected due to informalities. Claim 13 has been amended to correct the informalities. Claims 1, 2, 8, 13, 15, 20 and 24 have been amended. New claim 29 has been added and claim 7 has been cancelled. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Double Patenting Rejection

Claims 1-16 and 18-28 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-29 of copending Application no. 10/606,093 in view of Budnik, U.S. Patent No. 6,043,707 ("Budnik").

A terminal disclaimer is filed herewith. The terminal disclaimer should overcome the obviousness-type double patenting provisional rejection. Accordingly, withdrawal of this rejection is respectfully requested.

II. Rejection of Claims 1-2, 6, 11-14, 20 and 23 Under 35 U.S.C. §102(b)

Claims 1-2, 6, 11-14, 20 and 23 stand rejected under 35 U.S.C. §102(b) as being anticipated by Budnik. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 1 has been amended to recite that the power amplifier is an amplifier of a linear class type that operates as a constant class amplifier. Budnik discloses a variable-class amplifier that applies changes in bias and drive (supply) level to provide a supply type of envelope modulation at medium to high envelope amplitudes and allowing the amplifier to transition to highly efficient but non-linear classes of operation, such as Class C, D, E or F (Col. 4, ll. 9-14,

Col. 7, ll. 24-26). Each of the amplifiers (e.g., 494 of FIG. 6, 6 of FIG. 8, 106 of FIG. 9) disclosed in Budnik operate in a non-linear class, while applying supply type envelope modulation. In contrast, claim 1 recites a power amplifier of a linear class type that operates as a constant class amplifier that includes a mode selector that controls operation of the amplifier between a polar mode, an envelope tracking mode and a linear mode. Therefore, Budnik does not disclose each and every element of claim 1, and claim 1 is not anticipated by Budnik.

Claims 2, 6 and 11-14 depend directly or indirectly from claim 1, and contain each and every element of claim 1. Therefore, claims 2, 6 and 11-14 are not anticipated by Budnik.

Furthermore, claim 2, which depends from claim 1, has been amended to recite, the peak level signals being signals that have an amplitude equal to or greater than a threshold level substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the envelope tracking mode. Budnik discloses that the amplifier operated linearly with approximately constant supply voltage for envelope amplitude below 5 volts peak, in an envelope tracking mode for envelope amplitudes between 5 and 10 volts, and in an envelope modulation mode for envelope amplitudes approximately 10 volts peak (Col. 4, ll. 44-54). Budnik does not disclose the amplifier system operates in the linear mode for low level signals, the polar mode for peak level signals, and in the envelope tracking mode for signals between low level signals and peak level signals, the peak level signals being signals that have an amplitude equal to or greater than a threshold level substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the envelope tracking mode, as recited in amended claim 2. Therefore, Budnik does not anticipate amended claim 2.

Claim 20 has been amended to recite the amplifier system operates in the linear mode for input signal amplitudes below about the first threshold level, the polar mode for input signal amplitudes above about the second threshold level, and in the envelope tracking mode for input signal amplitudes between about the first threshold level and about the second threshold level, that the second threshold level having an amplitude substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the

envelope tracking mode. Budnik does not disclose a second threshold level having an amplitude substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the envelope tracking mode, as recited in amended claim 20. Therefore, Budnik does not disclose each and every element of claim 20, and claim 23, which depends therefrom, and thus claims 20 and 23 are not anticipated by Budnik.

For the reasons described above, claims 1-2, 6, 11-14, 20 and 23 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

III. Rejection of Claims 3-4, 15-17, 21, 24, 25, 27 and 28 Under 35 U.S.C. §103(a)

Claims 3-4, 15-17, 21, 24, 25, 27 and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Budnik in view of Gailus, *et al.*, U.S. Patent No. 6,449,465 ("Gailus").

Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 3 and 4 depend directly or indirectly from claim 1. The Examiner cites Gailus to teach the amplification technique in polar mode as recited in the claims 3, 16 and 21 and 24. The Examiner also cites Gailus to teach DACs that convert the input signal and supply signal from the analog to digital domain, as recited in claims 4 and 15. However, Gailus does not make up for the aforementioned deficiencies of Budnik with respect to claim 1. Therefore, claims 3 and 4 are not obvious over Budnik in view of Gailus.

Claim 15 has been amended to recite that the amplifier system operates in the linear mode for low amplitude level input signals below about a first threshold level, the polar mode for peak level input signals above about a second threshold level, and in the envelope tracking mode for signals between about the first threshold level and the second threshold level, the second threshold level having an amplitude substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the envelope tracking mode. Neither Budnik nor Gailus alone or in combination teach or suggest a second threshold level having an amplitude substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the envelope tracking mode, as recited

in amended claim 15. Therefore, Budnik in view of Gailus do not make obvious claims 15, and claims 16-17, which depend therefrom.

Claims 21 depends directly from claim 20. Gailus does not make up for the aforementioned deficiencies of Budnik with respect to claim 20. Therefore, claim 21 is not obvious over Budnik in view of Gailus.

Claim 24 has been amended to recite switching modes of operation of the power amplifier between envelope tracking mode, polar mode and linear mode based on a characteristic of the input signal relative to a first threshold level and a second threshold level, the second threshold level having an amplitude substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the envelope tracking mode. Neither Budnik nor Gailus alone or in combination teach or suggest the second threshold level having an amplitude substantially equal to a headroom voltage below a peak voltage of the input signal, the headroom voltage being associated with the envelope tracking mode, as recited in amended claim 24. Therefore, Budnik in view of Gailus do not make obvious claims 24, and claims 25, 27 and 28, which depend therefrom.

For the reasons described above, claims 3-4, 15-17, 21, 24, 25, 27 and 28 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Rejection of Claims 5, 18, 22 and 26 Under 35 U.S.C. §103(a)

Claims 5, 18, 22 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Budnik and Gailus further in view of Eidson, et al., U.S. Patent No. 6,681,101 ("Eidson"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

The Examiner cites Eidson to teach the recited delta sigma modulators. Eidson teaches that a sigma delta modulator provides a high-speed, one-bit stream to a control input of a synthesizer having an N, N+1 divider. The synthesizer output causes a voltage controlled oscillator to generate a phase-modulated carrier signal centered at a selected frequency (Co. 4, ll. 27-36). Eidson does not disclose that the digital supply and/or input signals are converted into

the analog domain directly at a desired radio transmission frequency, as recited in claims 5, 18, 22 and 26.

Furthermore, claims 5, 18, 22 and 26 depend from claims 1, 15, 20 and 24, respectively. Eidson does not make up for the aforementioned deficiencies of Budnik and Gailus with respect to claims 1, 15, 20 and 24. Therefore, claims 5, 18, 22 and 26 are not obvious over Budnik in view of Gailus and further in view of Eidson.

For the reasons described above, claims 5, 18, 22 and 26 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

V. New Claim 29

Claim 7 indicated as allowable has been cancelled and recast into independent claim 29. It is respectfully requested that claim 29 be allowed.

CONCLUSION

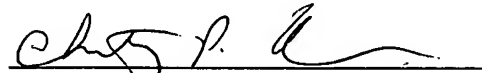
In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,

Date

8/29/05



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